

Attorney's Docket No.: 42390.P8533

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Jin Yang

Application No. 09/608,856

Filed: June 30, 2000

For: METHODS FOR PERFORMING  
GENERALIZED TRAJECTORY  
EVALUATION



Examiner: Unassigned

Art Unit: 2123

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Assistant Commissioner for Patents  
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Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231 on May 3 2002.

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If there are any additional charges, please charge Deposit Account No.  
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Respectfully submitted,

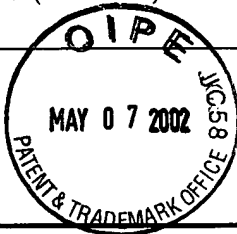
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Dated: 5-2-02

  
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Substitute for Form 1449A/PTO (Modified)		Attorney Docket No.: 42390.P8533	Application Number: 09/608,856
Sheet 1 of 4		First Named Inventor: Jin Yang	Examiner: Unassigned
		Filing Date: June 30, 2000	Art Unit: 2123



## U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (If known)			
		5,469,367		Puri et al	11-21-1995	
		5,491,639		Filkorn	02-13-1996	
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<b>Substitute for Form 1449A/PTO (Modified)</b> (use as many sheets as necessary)	<b>Attorney Docket No.:</b> 42390.P8533	<b>Application Number:</b> 09/608,856
Sheet 2 of 4	<b>First Named Inventor:</b> Jin Yang	<b>Examiner:</b> Unassigned
	<b>Filing Date:</b> June 30, 2000	<b>Art Unit:</b> 2123

**OTHER ART – NO PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation <sup>2</sup>
		BEREZIN, S. et al, "A Compositional Proof System for the Modal $\mu$ -Calculus and CCS," <i>Technical Report CMU-CS-97-105, Carnegie Mellon University, January 15, 1997</i>	
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		CHEN, Y. et al, "PBHD: An Efficient Graph Representation for Floating Point Circuit Verification," <i>Technical Report CMU-CS-97-134, Carnegie Mellon University, May 1997</i>	
		CHEUNG, S. et al, "Checking Safety Properties Using Compositional Reachability : Analysis," <i>ACM Transactions on Software Engineering and Methodology, Vol. 8, No. 1, January 1999, pages 49-78</i>	
		CHIODO, M. et al, "Automatic Compositional Minimization in CTL Model Checking," <i>Proceedings of 1992 IEEE/ACM International Conference on Computer-Aided Design, November, 1992, pages 172-178</i>	

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		CHOU, C., "The Mathematical Foundation of Symbolic Trajectory Evaluation," <i>International Conference on Computer-Aided Verification(CAV'99)</i> , Trento, Italy, July 1999 pp. 196-207, Proceedings of CAV'99, Lecture Notes in Computer Science #1633 (Editors: Nicolas Halbwachs & Doron Peled), Springer-Verlog, 1999	
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		CLARKE, E. M. et al, "Model Checking and Abstraction," <i>ACM Transactions on Programming Languages and Systems</i> , Vol. 16, No. 5, September 1994, pages 1512-1542	
		GRUMBERG, O., "Model Checking and Modular Verification," <i>ACM Transactions On Programming Languages and Systems</i> , Vol. 16, No. 3, May 1994, pages 843-871	
		JACKSON, D., "Exploiting Symmetry in the Model Checking of Relational Specifications," <i>Technical Report CMU-CS 94-219, Carnegie Mellon University</i> , December 1994	
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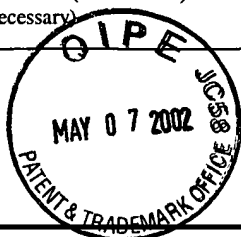
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		JAIN, A., "Formal Hardware Verification by Symbolic Trajectory Evaluation," <i>Carnegie Mellon University Ph.D. Dissertation</i> , July 1997	
		JAIN, S. et al, "Automatic Clock Abstraction from Sequential Circuits," <i>Proceedings of the 32<sup>nd</sup> ACM/IEEE Conference on Design Automation</i> , January 1995	
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		KERN, C. et al, "Formal Verification In Hardware Design: A Survey," <i>ACM Transactions on Design Automation of Electronic Systems</i> , Vol. 4, No. 2, April 1999, pages 123-193	
		KURSHAN, R. et al, "Verifying Hardware in its Software Context," <i>Proceedings of the 19<sup>th</sup> ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages</i> , February 1992, pages 742-749	
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		YEH, W. et al, "Compositional Reachability Analysis Using Process Algebra," <i>28<sup>th</sup> ACM/IEEE Design Automation Conference</i> , 1991	

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